CLAIMS

1. Communication device for processing outgoing and incoming packets, the device comprising:

a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal;

a mode line connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive mode; and

a control line to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

2. Communication device for processing an outgoing packet, the device comprising:

a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; and

a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the preceding signal processing units.

3. Communication device for processing an incoming packet, the device comprising:

a plurality of signal processing units connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal; and

a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the signal processing units following in the signal processing chain.

4. Device according to claim 1, wherein each signal processing unit comprises a multiplexing unit.

5. Device according to claim 2, wherein each signal processing unit comprises a multiplexing unit.

6. Device according to claim 3, wherein each signal processing unit comprises a multiplexing unit.

7. Device according to claim 1, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

8. Device according to claim 2, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

9. Device according to claim 3, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

10. Device according to claim 1, wherein each signal processing unit is connected via a logic unit to the control line.

11. Device according to claim 2, wherein each signal processing unit is connected via a logic unit to the control line.

12. Device according to claim 3, wherein each signal processing unit is connected via a logic unit to the control line.

13. Device according to claim 10, wherein the logic unit comprises an OR gate.

14. Device according to claim 11, wherein the logic unit comprises an OR gate.

15. Device according to claim 12, wherein the logic unit comprises an OR gate.

16. Device according to claim 1, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

17. Device according to claim 2, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

18. Device according to claim 3, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

19. Device according to claim 1, wherein each signal processing unit is usable for the transmit and receive mode.

20. Transceiver unit comprising a transceiver controller and a communication device, both transceiver controller and communication device being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; a mode line connected to each processing unit for switching each processing unit between a transmit mode and a receive mode; and a control line to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

21. Transceiver unit comprising a transceiver controller and a communication device, both being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; and a control line to which each signal processing unit is connected, the control line

communicating flow control information to at least one of the preceding signal processing units.

22. Transceiver unit comprising a transceiver controller and a communication device, both being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal; and a control line to which each signal processing unit is connected, the control line communicating flow information to at least one of the signal processing units following the signal processing chain.

23. Buffer system for storing data of a first processing unit and second processing unit comprising

a plurality of storage elements, each comprising a first storage unit and a second storage unit,

a plurality of switch subsystems for switching the storage elements between first and second modes, characterized by

in the first mode each first storage unit being addressable by the first processing unit and each second storage unit being addressable by the second processing unit, and

in the second mode each second storage unit being addressable by the first processing unit and each first storage unit being addressable by the second processing unit.

24. Buffer system according to claim 23, whereby each storage element comprises a plurality of cells.

25. Buffer system according to claim 23 further comprising a first address decoder for selecting one storage element for writing and reading data by the first processing unit.

26. Buffer system according to claim 23 further comprising a second address decoder for selecting one storage element for writing and reading data by the second processing unit.

27. Buffer system according to claim 23, whereby each switch subsystem comprises a plurality of access switches.

28. Baseband system comprising a communication device, wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; a mode line connected to each processing unit for switching each processing unit between a transmit mode and a receive mode; and a control line to which each signal unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

29. Baseband system comprising a buffer system, comprising a plurality of storage elements, each comprising a first storage unit and a second storage unit, a plurality of switch subsystems for switching the storage elements between first and second modes, characterized by in the first node each first storage unit being addressable by the first processing unit and each second storage unit being addressable by the second processing unit, and in the second mode each second storage unit being addressable by the first processing unit and each first storage unit being addressable by the second processing unit.

30. Method for storing data of a first processing unit and second processing unit in a buffer system comprising a plurality of storage elements, each storage element comprises a first storage unit and a second storage unit, the method comprising:
switching each storage element between first and second modes;
in the first mode addressing each first storage unit by the first processing unit and addressing each second storage unit by the second processing unit; and
in the second mode addressing each second storage unit by the first processing unit and addressing each first storage unit by the second processing unit.

31. Method according to claim 30 further comprising the step of selecting multiple storage elements and combining them to at least one storage block comprising a first storage block and a second storage block.

32. Method according to claim 31 further comprising the steps of

switching each storage block between first and second modes;

in the first mode addressing each first storage block by the first processing unit and addressing each second storage block by the second processing unit; and

in the second mode addressing each second storage block by the first processing unit and addressing each first storage block by the second processing unit.

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